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REPLY UNDER 37 C.F.R. § 1.116
EXPEDITED PROCEDURE
EXAMINING GROUP 2133

AP/RW
IFW

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application No.: 10/023,310
Filed: December 17, 2001
Inventor(s):
Chetana N. Keltcher, William
Alexander Hughes, Michael T.
Clark, and Bruce R. Holloway

Title: Using Microcode to Correct
ECC Errors in a Processor

§ Examiner: Torres, Joseph D.
§ Group/Art Unit: 2133
§ Atty. Dkt. No: 5500-75900
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I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on the date indicated below.

Lawrence J. Merkel

Printed Name

Signature

12/16/04

Date

**RESPONSE TO OFFICE ACTION OF
November 10, 2004**

Mailstop AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

This paper is submitted in response to the Office Action of November 10, 2004, to further highlight why the application is in condition for allowance.